

4.3mΩ, 40V, N-Channel Power MOSFET
SRT04N043LDTR-GS
General Description

The Sanrise SRT04N043LDTR-GS is a low voltage power MOSFET, fabricated using advanced split gate trench technology. The resulting device has extremely low on resistance, low gate charge and fast switching time, making it especially suitable for applications which require superior power density.

The SRT04N043LDTR-GS break down voltage is 40V and it has a high rugged avalanche characteristics.

The SRT04N043LDTR-GS is available in TO-252 package.

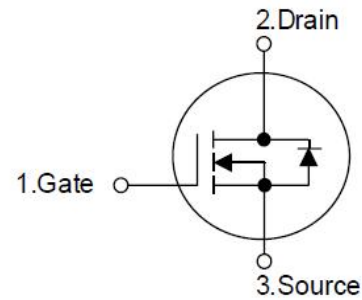
Symbol


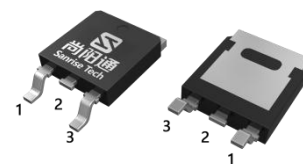
Figure 1 Symbol of SRT04N043LDTR-GS

Features

- Ultra Low
- $R_{DS(ON)}_{TYP} = 3.7m\Omega @ V_{GS} = 10V$.
- Ultra Low Gate Charge, $Q_g = 26nC$ typ.
- Fast switching capability
- Robust design with better EAS performance
- Non-automotive Qualified

Application

- Motor Driver
- E-Tools
- BMS
- Synchronous Rectifier

Package Type


TO-252

Figure 2 Package Type of SRT04N043LDTR-GS

Ordering Information

SRT04N043L□□-□		
Circuit Type	□	E: Lead Free
Package	□	GS: Green
D: TO-252	□	Blank: Tube
		TR: Tape & Reel

Package	Part Number	Marking ID	Packing Type
TO-252	SRT04N043LDTR-GS	SRT04N043LDGS	Tape&Reel

Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DSS}	40	V
Gate-Source Voltage		V_{GSS}	± 20	V
Continuous Drain Current, Package Limited	$T_C=25^{\circ}\text{C}$	I_D	50	A
	$T_C=100^{\circ}\text{C}$		50	
	$T_C=125^{\circ}\text{C}$		43	
Continuous Drain Current, Silicon	$T_C=25^{\circ}\text{C}$		104	
Pulsed Drain Current (Note 2)		I_{DM}	150	A
Power Dissipation ($T_C = 25^{\circ}\text{C}$)		P_D	93	W
Avalanche Destructive Energy, Single Pulse (Note 4)		E_{AS_Limit}	272	mJ
Avalanche Energy, Single Pulse (Note 3)		E_{AS}	36	mJ
Avalanche Energy, Repetitive (Note 2)		E_{AR}	0.1	mJ
Avalanche Current, Repetitive (Note 2)		I_{AR}	20	A
Continuous Diode Forward Current		I_S	50	A
Diode Pulse Current		$I_{S,PULSE}$	150	A
Operating Junction Temperature		T_J	175	$^{\circ}\text{C}$
Storage Temperature		T_{STG}	-55 to 175	$^{\circ}\text{C}$
Lead Temperature (Soldering, 10 sec)		T_{LEAD}	260	$^{\circ}\text{C}$

Note:

1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature
3. $I_{AS}=12\text{A}$, $V_{DD}=20\text{V}$, $R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$
4. $I_{AS}=33\text{A}$, $V_{DD}=20\text{V}$, $R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$

Thermal Resistance

Parameter	Symbol	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	R_{thJC}			1.6	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	R_{thJA}			62	

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Electrical Characteristics
 $T_J = 25^{\circ}\text{C}$, unless otherwise specified.

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Statistic Characteristics							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V, I _D =250uA	40			V
Zero Gate Voltage Drain Current		I _{DSS}	V _{DS} =40V, V _{GS} =0V			1	uA
Gate-Body Leakage Current	Forward	I _{GSSF}	V _{GS} =20V, V _{DS} =0V			100	nA
	Reverse	I _{GSSR}	V _{GS} =-20V, V _{DS} =0V			-100	
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =0.25mA	1.2	1.8	2.6	V
Static Drain-Source On-Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =20A		3.7	4.3	mΩ
Gate Resistance		R _G	f=1MHz, Open Drain		3.0		Ω
Dynamic Characteristics							
Input Capacitance		C _{ISS}	V _{DS} =20V, V _{GS} =0V, f=1MHz		1.8		nF
Output Capacitance		C _{OSS}			487		pF
Reverse Transfer Capacitance		C _{RSS}			31		pF
Effective output capacitance, energy related ^{NOTE5}		C _{O(er)}	V _{GS} =0V, V _{DS} =0...20V		760		pF
Effective output capacitance, time related ^{NOTE6}		C _{O(tr)}			936		
Turn-on Delay Time		t _{d(on)}	V _{DD} =20V, I _D =20A R _G =1.6Ω, V _{GS} =10V		13		ns
Rise Time		t _r			35		
Turn-off Delay Time		t _{d(off)}			40		
Fall Time		t _f			8		
Gate Charge Characteristics							
Gate to Source Charge		Q _{gs}	V _{DD} =20V, I _D =20A V _{GS} =0 to 10V		3.9		nC
Gate to Drain Charge		Q _{gd}			3.0		
Gate Charge Total		Q _g			26		
Gate Plateau Voltage		V _{plateau}			2.4		V
Gate Charge Total, sync FET		Q _g	V _{DD} =0.1V, V _{GS} =0 to 10V		24.6		nC
Reverse Diode Characteristics							
Drain-Source Diode Forward Voltage		V _{SD}	V _{GS} =0V, I _{SD} =20A		0.83	1.0	V
Reverse Recovery Time		t _{rr}	V _R =20V, I _F =20A dI _F /dt=100A/us		46		ns
Reverse Recovery Charge		Q _{rr}			70		nC
Peak Reverse Recovery Current		I _{rrm}			3.1		A

Note:

- $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 32V
- $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 32 V



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