

General Description

The Sanrise SRT10N230L is a low voltage power MOSFET, fabricated using advanced split gate trench technology. The resulting device has extremely low on resistance, low gate charge and fast switching time, making it especially suitable for applications which require superior power density and synchronous rectification.

The SRT10N230L break down voltage is 100V and it has a high rugged avalanche characteristics. The SRT10N230L is available in SOP-8 and TO-252 packages.

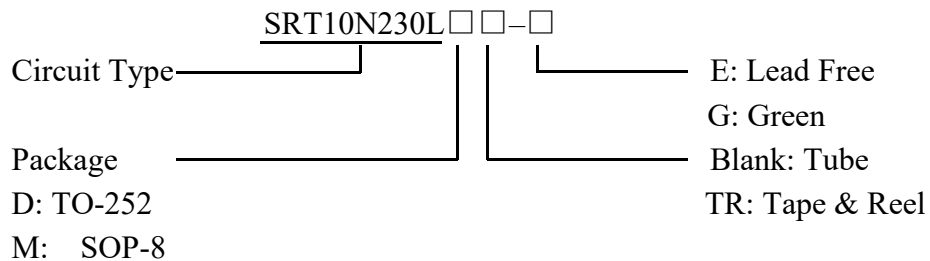
Features

- Ultra Low $R_{DS(ON_TYP)} = 18.5m\Omega @ V_{GS} = 10V$.
- Ultra Low Gate Charge, $Q_g = 11.3nC$ typ.
- Fast switching capability
- Robust design with better EAS performance
- Features Add Non-automotive Qualified

Application

- Charger/Adapter
- DC/DC Power Supply
- E-Tools
- BMS

Ordering Information



Symbol

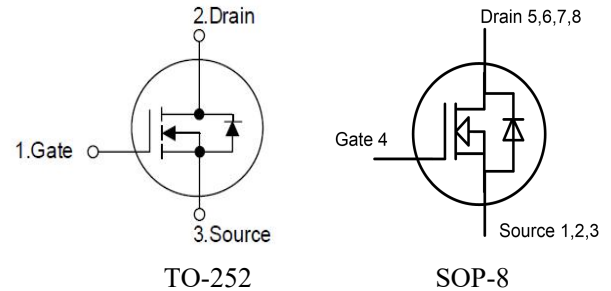


Figure 1 Symbol of SRT10N230L

Package Type

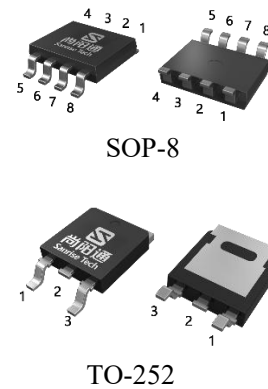


Figure 2 Package Type of SRT10N230L

Package	Part Number	Marking ID	Packing Type
SOP-8	SRT10N230LMTR-G	10N230LMG	Tape & Reel
TO-252	SRT10N230LDTR-G	SRT10N230LDG	Tape&Reel

Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit	
Drain-Source Voltage		V_{DSS}	100	V	
Gate-Source Voltage		V_{GSS}	±20	V	
Continuous Drain Current	$T_C=25^{\circ}C$	I_D	TO-252	30	A
	$T_A=25^{\circ}C$		SOP8	5.9	
	$T_C=100^{\circ}C$		TO-252	19	
	$T_A=100^{\circ}C$		SOP8	3.7	
Pulsed Drain Current (Note 2)		I_{DM}	87	A	
Power Dissipation ($T_C = 25^{\circ}C$)		P_D	36	W	
Avalanche Destructive Energy, Single Pulse (Note 4)		E_{AS_Limit}	56.25	mJ	
Avalanche Energy, Single Pulse (Note 3)		E_{AS}	12.25	mJ	
Avalanche Energy, Repetitive (Note 2)		E_{AR}	0.1	mJ	
Avalanche Current, Repetitive (Note 2)		I_{AR}	13	A	
Continuous Diode Forward Current		I_S	29	A	
Diode Pulse Current		$I_{S,PULSE}$	87	A	
Operating Junction Temperature		T_J	150	°C	
Storage Temperature		T_{STG}	-55 to 150	°C	
Lead Temperature (Soldering, 10 sec)		T_{LEAD}	260	°C	

Note:

1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature
3. $I_{AS} = 7.0A$, $V_{DD} = 50V$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}C$
4. $I_{AS_Limit} = 15.0A$, $V_{DD} = 50V$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}C$

Thermal Resistance

Parameter		Symbol	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Lead	SOP8	R_{thJL}			25	°C/W
Thermal Resistance, Junction-to-Case	TO-252	R_{thJC}			3.1	°C/W
Thermal Resistance, Junction-to-Ambient	SOP8	R_{thJA}			80	°C/W
Thermal Resistance, Junction-to-Ambient	TO-252	R_{thJA}			62	°C/W

Electrical Characteristics

$T_J = 25^\circ\text{C}$, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Statistic Characteristics							
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	100			V	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$			1	μA	
Gate-Body Leakage Current	Forward	$I_{GSSF}, V_{GS}=20V, V_{DS}=0V$			100	nA	
	Reverse	$I_{GSSR}, V_{GS}=-20V, V_{DS}=0V$			-100		
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=0.25mA$	1.2	1.8	2.4	V	
Static Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=4.5V, I_D=15A$		25.9	34	$m\Omega$	
Static Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=15A$		18.5	23	$m\Omega$	
Gate Resistance	R_G	$f=1MHz, \text{Open Drain}$		1.3		Ω	
Dynamic Characteristics							
Input Capacitance	C_{ISS}	$V_{DS}=50V, V_{GS}=0V, f=1MHz$		749		pF	
Output Capacitance	C_{OSS}				218		pF
Reverse Transfer Capacitance	C_{RSS}				4		pF
Effective output capacitance, energy related <small>NOTE5</small>	$C_{O(er)}$	$V_{GS}=0V, V_{DS}=0\dots 60V$		295		pF	
Effective output capacitance, time related <small>NOTE6</small>	$C_{O(tr)}$				347		
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=50V, I_D=15A, R_G=3.0\Omega, V_{GS}=10V$		5.6		nS	
Rise Time	t_r			4.1			
Turn-off Delay Time	$t_{d(off)}$			12.1			
Fall Time	t_f			2.8			
Gate Charge Characteristics							
Gate to Source Charge	Q_{gs}	$V_{DD}=50V, I_D=15A, V_{GS}=0 \text{ to } 4.5V$		2.4		nC	
Gate to Drain Charge	Q_{gd}			2.0			
Gate Charge Total	Q_g			5.6			
Gate Charge Total	Q_g	$V_{DD}=50V, I_D=15A, V_{GS}=0 \text{ to } 10V$		11.3		nC	
Gate Charge Total, sync FET	Q_g	$V_{DD}=0.1V, V_{GS}=0 \text{ to } 10V$		10.0		nC	
Reverse Diode Characteristics							
Drain-Source Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_{SD}=15A$		0.9	1.1	V	
Reverse Recovery Time	t_{rr}	$V_R=50V, I_F=15A, dI_F/dt=100A/\mu s$		21		nS	
Reverse Recovery Charge	Q_{rr}				17		nC
Peak Reverse Recovery Current	I_{rrm}				1.6		A

Note:

- $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 60V
- $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 60 V



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