

General Description

The Sanrise SRT10N160L is a low voltage power MOSFET, fabricated using advanced split gate trench technology. The resulting device has extremely low on resistance, low gate charge and fast switching time, making it especially suitable for applications which require superior power density and synchronous rectification.

The SRT10N160L break down voltage is 100V and it has a high rugged avalanche characteristics. The SRT10N160L is available in DFN5*6 and SOP-8 and TO-252 packages.

Features

- Ultra Low $R_{DS(ON)}$
 $R_{DS(ON_TYP)} = 13.5m\Omega @ V_{GS} = 10V.$
 $R_{DS(ON_TYP)} = 18.3m\Omega @ V_{GS} = 4.5V$
- Ultra Low Gate Charge,
 $Q_g = 16.1nC \text{ typ} @ V_{GS} = 10V.$
 $Q_g = 8.0nC \text{ typ} @ V_{GS} = 4.5V.$
- Fast switching capability
- Robust design with better EAS performance

Application

- Charger/Adapter
- DC/DC Power Supply
- E-Tools
- BMS

Symbol

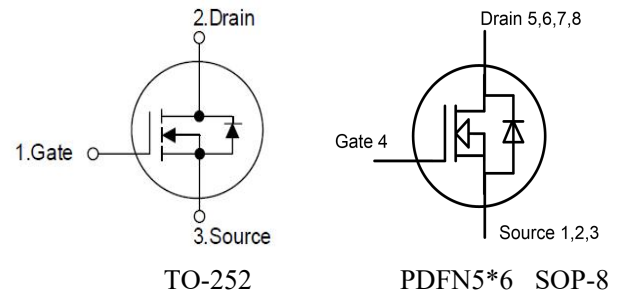


Figure 1 Symbol of SRT10N160L

Package Type

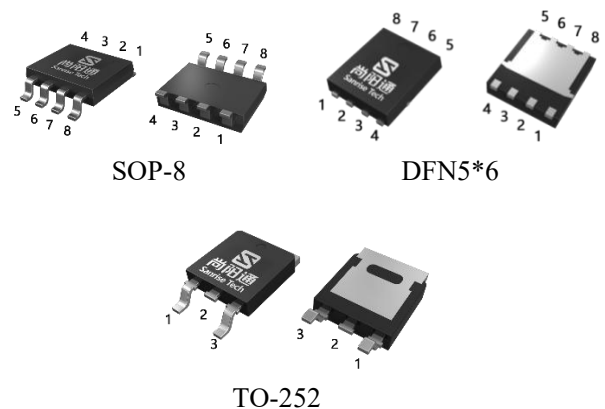
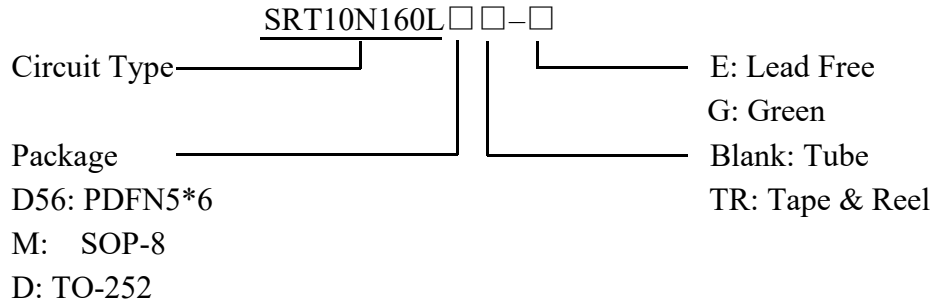


Figure 2 Package Type of SRT10N160L

16mΩ, 100V, N-Channel Power MOSFET
SRT10N160L
Ordering Information


Package	Part Number	Marking ID	Packing Type
PDFN5*6	SRT10N160LD56TR-G	SRT10N160LD56G	Tape & Reel
SOP-8	SRT10N160LMTR-G	10N160LMG	Tape & Reel
TO-252	SRT10N160LDTR-G	SRT10N160LDG	Tape & Reel

Absolute Maximum Ratings

Parameter		Symbol	Rating		Unit
Drain-Source Voltage		V_{DSS}	100		V
Gate-Source Voltage		V_{GSS}	±20		V
Continuous Drain Current	$T_C=25^{\circ}C$	I_D	PDFN5*6	40	A
	$T_C=25^{\circ}C$		TO252	41	
	$T_A=25^{\circ}C$		SOP-8	7.1	
	$T_C=100^{\circ}C$		PDFN5*6	25	
	$T_C=100^{\circ}C$		TO252	26	
	$T_A=100^{\circ}C$		SOP-8	4.5	
Pulsed Drain Current (Note 2)		I_{DM}	PDFN5*6	120	A
			TO252	123	
			SOP-8	21	
Avalanche Energy, Single Pulse (Note 3)		E_{AS}	40		mJ
Avalanche Energy, Repetitive (Note 2)		E_{AR}	0.1		mJ
Avalanche Current, Repetitive (Note 2)		I_{AR}	15		A
Continuous Diode Forward Current		I_S	40		A
Diode Pulse Current		$I_{S,PULSE}$	120		A
Operating Junction Temperature		T_J	150		°C
Storage Temperature		T_{STG}	-55 to 150		°C
Lead Temperature (Soldering, 10 sec)		T_{LEAD}	260		°C

Note:

1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature
3. $I_{AS}= 15.0A$, $V_{DD}= 50V$, $R_G= 25\Omega$, Starting $T_J= 25^{\circ}C$

Thermal Resistance

Parameter		Symbol	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	PDFN5*6	R_{thJC}			2.5	°C/W
Thermal Resistance, Junction-to-Case	TO252	R_{thJC}			2.3	°C/W
Thermal Resistance, Junction-to-Lead	SOP8	R_{thJL}			25	°C/W
Thermal Resistance, Junction-to-Ambient	PDFN5*6	R_{thJA}			50	°C/W
Thermal Resistance, Junction-to-Ambient	TO252	R_{thJA}			62	°C/W
Thermal Resistance, Junction-to-Ambient	SOP8	R_{thJA}			80	°C/W

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Electrical Characteristics

 T_J = 25 °C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Statistic Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	100			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V			1	uA
Gate-Body Leakage Current	Forward	I _{GSSF}	V _{GS} =20V, V _{DS} =0V		100	nA
	Reverse	I _{GSSR}	V _{GS} =-20V, V _{DS} =0V		-100	
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =0.25mA	1.2	1.8	2.4	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =4.5V, I _D =10A		18.3	23.5	mΩ
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A		13.5	16	mΩ
Gate Resistance	R _G	f=1MHz, Open Drain		1.0		Ω
Dynamic Characteristics						
Input Capacitance	C _{ISS}	V _{DS} =50V, V _{GS} =0V, f=1MHz		1000		pF
Output Capacitance	C _{OSS}			310		pF
Reverse Transfer Capacitance	C _{RSS}			6		pF
Effective output capacitance, energy related ^{NOTE5}	C _{O(er)}	V _{GS} =0V, V _{DS} =0...60V		422		pF
Effective output capacitance, time related ^{NOTE6}	C _{O(tr)}			497		
Turn-on Delay Time	t _{d(on)}	V _{DD} =50V, I _D =20A R _G =3.0Ω, V _{GS} =10V		5.9		nS
Rise Time	t _r			3.9		
Turn-off Delay Time	t _{d(off)}			14.8		
Fall Time	t _f			3.1		
Gate Charge Characteristics						
Gate to Source Charge	Q _{gs}	V _{DD} =50V, I _D =20A V _{GS} =0 to 4.5V		3.5		nC
Gate to Drain Charge	Q _{gd}			2.8		
Gate Charge Total	Q _g			8.0		
Gate Charge Total	Q _g	V _{DD} =50V, I _D =20A V _{GS} =0 to 10V		16.1		nC
Gate Charge Total, sync FET	Q _g	V _{DD} =0.1V, V _{GS} =0 to 10V		14.3		nC
Reverse Diode Characteristics						
Drain-Source Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _{SD} =20A		0.89	1.1	V
Reverse Recovery Time	t _{rr}	V _R =50V, I _F =20A dI _F /dt=100A/us		25		nS
Reverse Recovery Charge	Q _{rr}			24		nC
Peak Reverse Recovery Current	I _{rrm}			1.9		A

Note:

 5. C_{O(er)} is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 60V

 6. C_{O(tr)} is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 60 V



Sanrise Technology Limited Company

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Main Site:

- Headquarter

Shenzhen Sanrise Technology Co., LTD.

A1206, Skyworth building, No. 008, gaoxinnan 1st Road,
Gaoxin District, Yuehai street,, Nanshan District, ShenZhen,
P.R.China

Tel: +86-755-22953335

Fax: +86-755-22916878

- Shanghai Office

Sanrise Technology Limited Company

Rm.401, Building B, No. 666, Zhangheng Road,
Zhangjiang Hi-Tech Park, Shanghai, P.R.China

Tel: +86-21-68825918